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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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10/799,537

03/12/2004

Li-Kong Wang

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EXAMINER

TRA, ANH QUAN

ART UNIT

PAPER NUMBER

2816

MAIL DATE

DELIVERY MODE

12/31/2008

PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No. 10/799,537	Applicant(s) WANG ET AL.	
	Examiner QUAN TRA	Art Unit 2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 18 November 2008.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-10 and 12 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-10 and 12 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

1. This office action is in response to the amendment filed 11/18/08. New grounds of rejection are introduced as necessitated by amendment.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. Claims 1-10 and 12 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. The original specification fails to teach "each local DC voltage generator receives from said power control unit a different one of plurality of power control signals for controlling the power supplied to the local DC generator and its at least one unit of the plurality of subsystems and receives from said clock control unit a a different one of plurality clock control signals for controlling the timing of the local DC generator and its at least one unit of the plurality of subsystems. As understood from pages 6 and 7 of the specification, the power control signal and clock control signal are for enable/disable the local DC generators, not controlling the power supplied to the local DC generator or controlling the timing of the local DC generators.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and

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the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claims 1-10 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Pasternak (USP 6577535) in view of Ong (USP 6732304) and Drouot (USP 5796285).

The combination of Pasternak and Ong's references shows plurality of DC voltage generators (the CP in 304 and 310) comprising all elements of the claims (see the rejection in previous office action) except for the detail of each charge pump circuit. However, Drouot's figure 1 shows a low cost charge pump circuit. Therefore, it would have been obvious to one having ordinary skill in the art to use Drouot's charge pump circuit for each of Pasternak's charge pumps for the purpose of saving cost. Thus, the modified Pasternak's figure 3A further shows a power control unit (circuit in Pasternak's 302 that generates signal CS0 and inverter 362) for generating a plurality of power control signals (CS0 and the output of 362); a clock control unit (circuit in 302 that generates signal CS1 and inverter 364) for generating a plurality of clock control signals (CS1 and output of 364); and a plurality of local DC voltage generators (the CP in 304 and 310) distributed throughout the SOC chip, each local DC voltage generator independently supplying voltage to at least one unit of the plurality of subsystems, each local DC voltage generator including at least one regulator system (Drouot's 5) incorporated in the local DC voltage generator, wherein each local DC voltage generator receives from said power control unit a different one of the plurality of power control signals for controlling the power supplied to the local DC generator and its at least one unit of the plurality of subsystems and receives from said clock control unit a different one of the plurality of clock control signals for controlling the timing of the local DC generator, said clock control signal also supplied to and its at least one unit of the plurality of subsystems *[outputs of Pasternak's figure 3B, which is controlled by one of the inputs of each AND gates (the power control signal), can be considered as power signals which are supplied to the charge pumps and memory circuits in figure 3A. The*

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other input of each AND gates in figure 3b (the clock control signal) controls the on/off times of the charge pumps and memory circuits in figure 3a]; AND gate (Pasternak's 352 or 354); first to third transistors (Drouot's 16, 12, 11) connected as claimed, wherein the power control signal and the clock control signal controlling one of the local DC voltage generators also control the unit associated with the one of the local DC voltage generators, wherein each local DC voltage generator is individually controlled in accordance with its respective power control signal and clock control signal, and wherein each of the units is individually provided with power only from an associated local DC voltage generator.

Conclusion

3. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to QUAN TRA whose telephone number is 571-272-1755. The examiner can normally be reached on 8:00 AM - 5:00 PM.

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If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lincoln Donovan can be reached on 571-272-1740. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/QUAN TRA/
Primary Examiner, Art Unit 2816